L-DACS1 PHYSICAL LAYER LABORATORY DEMONSTRATOR

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Abstract

In this paper, an L-DACS1 physical layer laboratory demonstrator is presented which has been implemented recently in FPGA technology by the German Aerospace Center (DLR). The main goal of this lab demonstrator is to perform first compatibility measurements between L-DACS1 and legacy L-band systems where interference from L-DACS1 towards the legacy systems as well as interference from the legacy systems onto the L-DACS1 receiver is considered. The lab demonstrator is already implemented up to the first intermediate frequency at 10.7 MHz. The radio frontend for up-/down-conversion to/from the L-band is scheduled to be delivered in May this year. First compatibility tests are planned to take place in the labs of the German ATC authority DFS this summer. Using real hardware equipment, these tests will give valuable insight into the L-band coexistence issue and possible deployment scenarios.

1. Introduction

Within the future communications study (FCS) jointly carried out by Eurocontrol and the FAA, two candidates for the future L-band Digital Aeronautical Communications System (L-DACS) have been identified. The first candidate termed L-DACS1 is a broadband system employing Orthogonal Frequency-Division Multiplexing (OFDM) as modulation scheme and separating forward and reverse link by frequency-division duplex (FDD), whereas the second candidate termed L-DACS2 is a narrowband single-carrier system utilizing time-division duplex (TDD) as duplex scheme. The FCS has recommended follow-on activities in order to further specify the proposed L-DACS options and validate their coexistence with other L-band systems with the goal to finally decide for one candidate as soon as possible.

Within a Eurocontrol study finalized last year, both L-DACS options have been specified in detail. The specifications are publically available from the Eurocontrol website [1]. A detailed description of the main features of the L-DACS1 physical layer as defined within the specification was presented at last year's ICNS conference [2]. Having available complete specifications for the L-DACS candidates, the next step is to prove the coexistence of L-DACS with the legacy systems operated in L-band. The L-band is used by navigation and surveillance as well as military communications systems. The main L-band navigation and surveillance systems are the Distance Measurement Equipment (DME), the Secondary Surveillance Radar (SSR), and the Universal Access Transceiver (UAT), whereas the Joint Tactical Information Distribution System (JTIDS) is the main military communications system used in L-band.

Current work on L-DACS is performed under the framework of SESAR. The corresponding SESAR project P15.2.4 "Future Mobile Data Link System Definition" has started activities on L-DACS within an Early Task mid of February this year. Main goals of this Early Task are the refinement of L-DACS specifications and the development of both evaluation criteria for L-band compatibility testing and the L-DACS evaluation testbed. Besides the SESAR activities, DLR has already started to implement an L-DACS1 physical layer laboratory demonstrator in FPGA technology based on the current L-DACS1 specification [3]. The demonstrator enables investigations of both the influence of the L-DASC1 waveform on legacy L-band systems and the interference from legacy L-band systems on the L-DACS1 receiver. These investigations are especially of interest for the so-called "inlay" deployment scenario, where L-DACS1 and DME share the L-band as common spectrum resource by implementing L-DACS1 channels of approximately 500 kHz bandwidth between two adjacent DME channels. According to [3], the inlay deployment is not the only possible L-DACS1 deployment scenario. However, it is the most efficient approach and, thus, shall be investigated first before considering alternative deployment options.

Since proof of L-band coexistence is the main scope of the demonstrator, the focus is on physical layer implementation in FPGA technology. As will be explained herein, the demonstrator set-up comprises a complete implementation of the physical layer of the L-DACS1 transmitter. The receiver hardware design is capable of continuously recording the received signal. A software receiver may then be used to process the resulting data.

This paper is organized as follows. The L-DACS1 physical layer as specified in [3] is briefly reviewed in Section 2. Section 3 details the properties and capabilities to be implemented for the laboratory demonstrator. Section 4 explains the actual demonstrator implementation and briefly introduces the hardware used for it. First measurements of the generated IF transmit signal spectrum and modulation fidelity are presented in Section 5. Section 6 will conclude this paper with an outlook on planned compatibility tests between legacy systems and L-DACS1 to be performed at the labs of the German ATC authority DFS this summer.

2. L-DACS1 Physical Layer

As it supports a more detailed understanding of the demonstrator's tasks, we would like to summarize the main characteristics of L-DACS1, focusing on its physical layer. It should be noted that L-DACS1 has an air-ground (A/G) and an air-air (A/A) mode of operation, which use different technologies on the physical and other layers. So far, only the A/G mode has been specified in detail and in this paper, only the A/G mode is considered.

L-DACS1 A/G is a cellular communications system comprising a network of ground stations (GS) providing radio links to mobile users termed airborne stations (AS). It employs orthogonal frequency-division multiplexing (OFDM) as modulation scheme. The nominal Fast Fourier Transform (FFT) length is $N_{FFT} = 64$ and the subcarrier spacing is $\Delta f = (5/512)\text{MHz}$ (about 9.8 kHz). A maximum of $N_u = 50$ subcarriers are used for transmission, with one DC-subcarrier separating two groups of 25 subcarriers. All unused subcarriers, including the DC subcarrier, are set to zero. This results in an effective bandwidth of 498.05kHz, which can be considered broadband compared to legacy aeronautical communications systems.

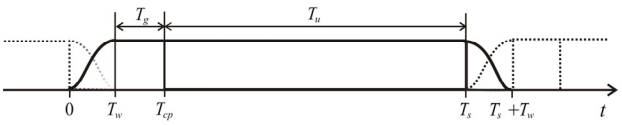

Figure 1: Cyclic extension and TX windowing.

The useful OFDM symbol duration of $T_u = 1/\Delta f = 102.4\mu\text{s}$ is extended by a cyclic prefix of $T_{cp} = 17.6\mu\text{s}$, comprising $T_g = 4.8\mu\text{s}$ of guard time and $T_w = 12.8\mu\text{s}$ of rising window flank, as well as by a cyclic suffix of T_w for the falling window flank (see Figure 1, taken from [3]). As the window flanks of consecutive OFDM symbols overlap, the total L-DACS1 OFDM symbol duration is $T_s = 120\mu\text{s}$. The transmit windowing multiplies each extended OFDM symbol with a raised-cosine window (parameter $\alpha = 0.107$ [3]). It reduces out-of-band radiations to levels below the spectral mask defined for L-DACS1 in [3]. The spectral properties of L-DACS1 are further analyzed together with measurements in Section 5 of this paper.

In L-DACS1, the ground-to-air link (GS to AS) is called the forward link (FL) and the inverse direction (AS to GS) is termed reverse link (RL). FL and RL are separated by frequency-division duplex (FDD), with a spacing of 69MHz. The FL is a continuous OFDM stream with logical channels for broadcast and for individual users. The RL uses orthogonal frequency- / time-division multiple access (OFDMA/TDMA) to dynamically assign tiles of subcarriers on a time-frequency map to users. This allows to keep the L-DACS1 transmit duty cycle of each individual aircraft at an acceptable, low level.

2.1 L-DACS1 Framing

L-DACS1 FL transmissions consist of frames, where a frame is a predefined structure of OFDM symbols. An example can be seen in Figure 2 (taken from [3]), where each row of the grid represents one OFDM symbol and the individual squares represent modulation symbols on the subcarriers of the OFDM symbol. Each frame begins with a number

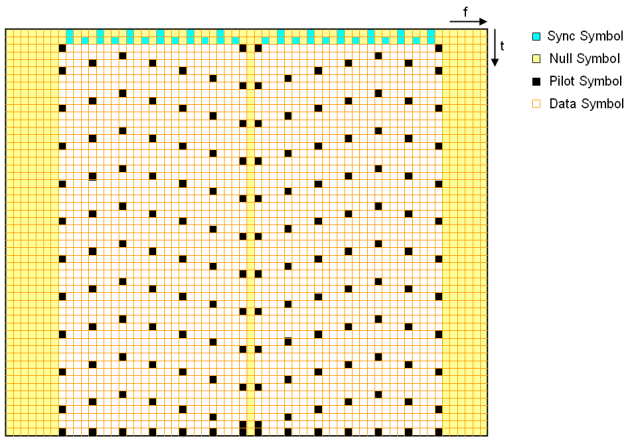

Figure 2: FL data/CC frame.

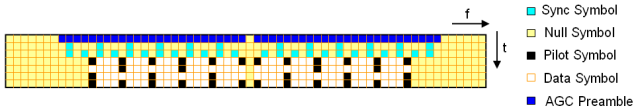

Figure 3: RL random access frame.

of predefined header ODFM symbols, of which three different types exist in L-DACS1: two different synchronization OFDM symbols and one automatic gain control (AGC) preamble (only used in the RL). Following the header, a data section is transmitted, which is defined by its length in OFDM symbols, the numbers of used subcarriers in the halves of the spectrum below and above the DC carrier (always 25 each for the FL), and the position and content of predefined pilot symbols in the individual OFDM symbols. The latter are needed for channel estimation in the receiver.

In the reverse link, random access (RA) for net entry is enabled by the transmission of RA frames as depicted in Figure 3 (taken from [3]) during special random access opportunity periods. They can be described by the same parameters as FL frames. Note that in this case, the number of used subcarriers is reduced to 21 on each side of the DC carrier. The remainder of the RL is organized in data or control sections consisting of tiles, as well as groups of header OFDM symbols which may precede these sections. Each header OFDM symbol or tile can be dynamically assigned to users by the base station for maintaining synchronization or transmitting control or user data. One such section, consisting of 6 tiles and preceded by 6 header OFDM symbols, is shown in Figure 4 (taken from [3]). Each tile uses 25 subcarriers of 6 consecutive OFDM symbols and is located in the spectrum

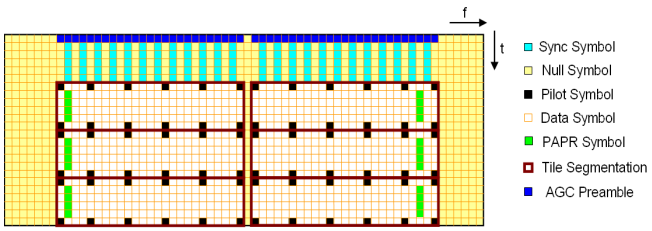

Figure 4: RL header symbols and section.

either below or above the DC subcarrier. Note that tiles in the RL contain peak to average power ratio (PAPR) reduction subcarriers. Those subcarriers are discarded in the receiver. Their content may be chosen by the transmitter in an implementation specific way to reduce peaks in the transmit signal.

The elements of L-DACS1 framing that have just been introduced are organized in a repetitive 240 ms Super-Frame structure as shown in Figure 5 (taken from [3]). Super-Frames are further divided into four entities termed Multi-Frames, preceded by three broadcast (BC) frames in the FL and, simultaneous to that, by the random access (RA) timeslots in the RL. A Multi-Frame is made up of the frames, sections of tiles and groups of header OFDM symbols as described in the previous paragraphs. It is further detailed in Figure 6 (also taken from [3]). In Figures 5 and 6, the abbreviations DC and CC denote dedicated and common control information, respectively. User data is marked as “Data”. Please see [3] for a more detailed description.

2.2 Coding and Subcarrier Modulation

L-DACS1 adapts to varying quality of the physical channel by supporting a number of adaptive coding and modulation options (ACM). They all rely on an outer Reed-Solomon (RS) code followed by a convolutional code of basic rate 1/2 with two optional puncturing schemes to achieve higher convolutional code rates of 2/3 or 3/4. The employed RS code is a systematic code from Galois Field (GF) 2^8 with a variable number of check symbols and code words shortened to the desired length. The convolutional code polynomials are (171, 133) in octal notation. After coding, the bits of each codeword are interleaved and mapped to modulation symbols using quaternary phase shift keying (QPSK), 16-quadrature amplitude modulation (16-QAM) or 64-QAM. Details on

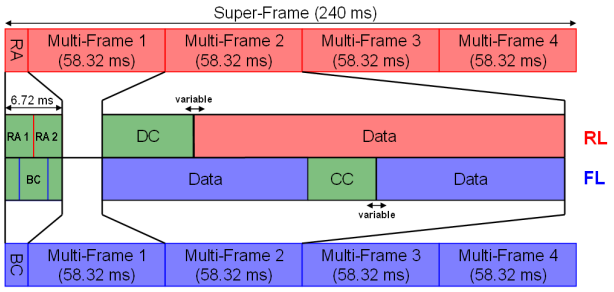

Figure 5: Super-Frame structure.

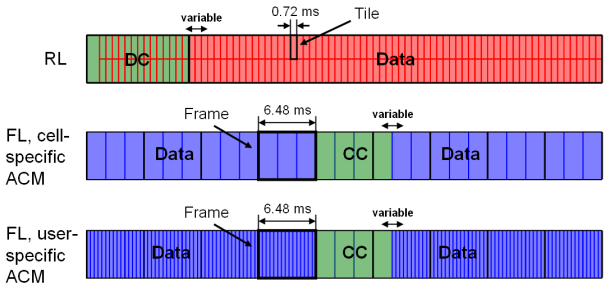

Figure 6: Multi-Frame structure.

coding, interleaving, symbol mapping and the supported combinations can be found in [3].

For convenience, the main OFDM parameters relevant for the demonstrator are summarized in Table 1.

3. Demonstrator Requirements

The objectives of our demonstrator development are twofold. First, the effects of L-DACS1 signals on existing systems in the L-band are to be analyzed using a realistic setup, i.e. actual hardware. This will allow to establish the conditions under which coexistence of L-DACS1 with such systems is possible, for example the necessary spatial and spectral separation. Secondly, the robustness of L-DACS1 against interference from other systems is to be demonstrated and assumptions regarding the bit error rate (BER) and minimum required signal level have to be proven.

In order to achieve this, the transmitter (TX) has to be able to generate all L-DACS1 frame types for the FL and all frame types, header OFDM symbols and sections for the RL. It should be able to output any sequence composed of the above types of signals that will also occur in the final L-DACS 1 system. Furthermore, support of all ACM options defined in [3] is desired. For later comparison of transmitted and received data, i.e.

Table 1: L-DACS1 OFDM parameters

Parameter description	Value
Nominal FFT length (N_{FFT})	64
Subcarrier spacing (Δf)	5/512 MHz
Used subcarriers (N_u)	50 (max.)
Effective bandwidth	498.05 kHz
OFDM symbol duration (T_u)	102.4 µs
Cyclic prefix, total Guard time Window flank	16.6 µs 4.8 µs 12.8 µs
Total OFDM symbol duration (T_s)	120 µs

BER evaluation, it has to be possible to fill transmit sequences with arbitrary, predefined data, e.g. read from a file. In order to facilitate accurate BER measurements, large amounts of user data have to be transmitted in an automated way in one experiment, e.g. all in one long sequence.

In the L-DACS1 specification [3], the receiver (RX) algorithm is not defined in detail, and can thus be considered implementation-specific. Depending on how exactly the system will be deployed in the L-band (cf. [2]), the RX will have to operate under significant interference conditions. As the deployment concept has not yet been decided and so far, only theoretical analysis of the interference has been done, no detailed interference model is available. Therefore, the demonstrator's RX signal processing must stay flexible and easy to adapt to refined RX algorithms. This can be achieved by implementing as much of it as possible in software. The hardware part only has to implement filtering and down-conversion into complex (I/Q) baseband samples, which can then be stored, e.g. on the hard disk of a host computer, to allow later software processing. Similar to the TX, the RX should be able to record long, continuous sequences for the purpose of accurate BER measurements. The output of such a data grabbing RX can also be a great aid in the development and testing of new RX algorithms.

As the development of the described L-DACS1 demonstrator began prior to the finalization of the L-DACS1 specification, a further design goal was to keep the implementation of all signal processing components as flexible as possible, in

order to allow easy parameter modification (e.g. framing structure, coding parameters). Another reason for this is the planned re-use of as much of the implementation as possible in a data link for research aircraft of the German Aerospace Center.

4. Implementation Details

The L-DACS1 physical layer laboratory demonstrator consists of signal processing units for RX and TX, as well as of a radio frequency (RF) frontend (see Figure 7). The main interface between those stages consists of the analogue TX and RX signals on an intermediate frequency (IF) of 10.7MHz, down-converted from the L-band and amplified by the frontend for RX and delivered to the frontend for TX. This paper focuses on the implementation of signal processing in the respective RX and TX units, up to the aforementioned IF level. A short outline of the frontend will be given at the end of this section.

For the purpose of signal processing in experimental implementations, two identical FPGA-based systems have been purchased by the German Aerospace Center from an external supplier. As shown in Figure 8, the compact-PCI platforms contain a host PC, two processing boards, a digital to analogue (D/A) converter board and an analogue to digital (A/D) converter board. The processing boards rely on an Altera Stratix II GX FPGA for arbitrary user designs. Memory is also provided, together with hardware, firmware and software for a PCI interface between boards and the host computer. This interface provides software functions for sending data from the host to a board and vice-versa. On the processing FPGA, by an already existing firmware component, data from the host computer is made available via an Avalon-Streaming (AVST) interface [4], which in this case can be thought of as a first in first out (FIFO) memory. This interface firmware component also accepts data via AVST and transfers it to the host where it is available through the software functions. Furthermore, it is possible to setup data streams from a processing board to the D/A converter board and from the A/D converter board to a processing board.

As indicated in Table 2, the D/A and A/D converters both support 2 channels with a resolution of 14bits. The maximum conversion rates supported

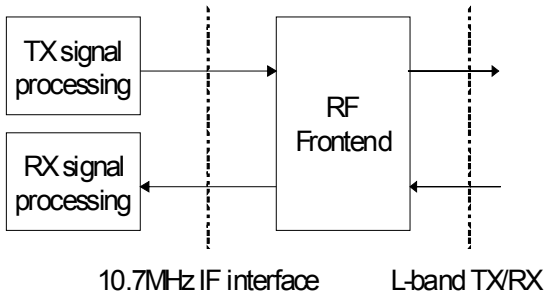

Figure 7: Demonstrator setup.

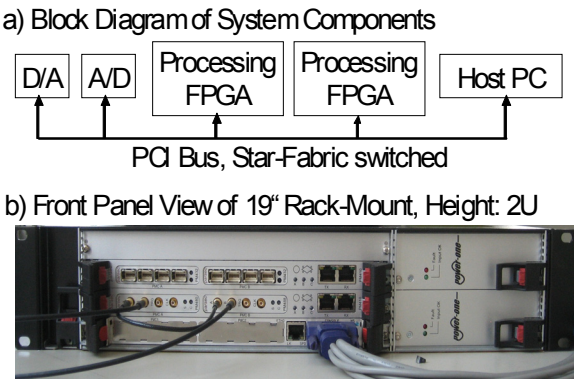

Figure 8: Signal processing system.

are 150MHz and 105MHz for D/A and A/D, respectively. For the L-DACS1 demonstrator, the sampling clocks have both been set to 30MHz, which is sufficient for the desired IF and signal bandwidth. This reduction minimizes the necessary bandwidth between processing boards and converter boards. Image rejection in the TX is no problem at this sampling rate because the employed D/A converter chip internally performs a numerical interpolation to two times the input rate. The Stratix II FPGAs on the processing boards are clocked at 100MHz.

Table 2: Signal processing system parameters

Parameter description	Value
Processing board FPGA Clock	Stratix II GX 100 MHz
D/A Converter channels Resolution Clock used / max	2 14 bits 30 MHz / 150MHz
A/D Converter channels Resolution Clock used / max	2 14 bits 30 MHz / 105MHz
System interconnection PCI Clock	PCI / Star-Fabric 66 MHz

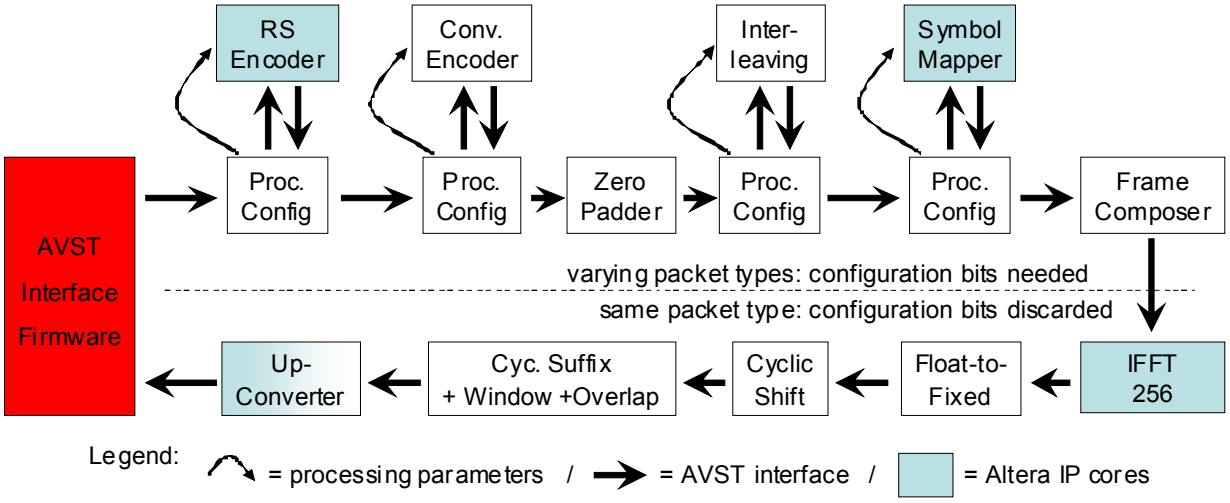

Figure 9: Block diagram of transmitter signal generation architecture.

In the following subsections, the L-DACS1 demonstrator FPGA design will be described. For this implementation, Altera DSP Builder version 9.0 was used. Simulations were performed in DSP Builder, i.e. Matlab/Simulink, and in Mentor Graphics ModelSim. Altera Quartus II version 9.0 was used for compiling the design together with the already existing AVST interface firmware.

4.1 Transmitter FPGA Design

The transmitter signal processing FPGA design that had to be implemented for the physical layer laboratory demonstrator receives Avalon-Streaming packets at its input containing all parameters and data for a sequence of L-DACS1 frames. This is enabled by the AVST interface firmware of the signal processing systems and software running on the host PC. From the received packets, the aforementioned IF signal has to be generated, along with an envelope signal and an activation signal for the RF amplifier termed push-to-talk (PTT). The envelope signal is needed by the frontend for accurate TX power control. The generated signals have to be sent back to the AVST interface firmware, which for the TX has to be configured to transmit data to the D/A board. To accomplish these tasks, functional blocks are connected via AVST into a processing chain. Apart from some details like packet reformatting, this chain is made up of the following blocks: RS encoder, convolutional encoder, zero padder, interleaver, symbol mapper, frame composer, inverse Fast Fourier Transform (IFFT), fixed-point converter, cyclic shift, cyclic suffix addition with windowing and finally, the up-converter. The chain is depicted in Figure 9. Zero padding prior to interleaving is necessary, as some code words are not of the exact same length as the interleaving scheme (also described in [3]). As the IFFT outputs floating-point numbers, a conversion to fixed-point must be performed. Furthermore, as described in Section 2 of this paper, cyclic extension in L-DACS1 involves both prefix and suffix. This can be represented as a cyclic shift of the OFDM symbol followed by the attachment of a suffix only, and has been implemented in this way. Note that the block appending the suffix also multiplies each OFDM symbol with the necessary TX window and adds together the overlapping window flanks of consecutive OFDM symbols. The concept used in terms of sampling rate relies on a four-times oversampling in the IFFT with respect to the nominal transform length (cf. Table 1), which leads to a transform length of $4 \cdot N_{FFT} = 256$ and a complex baseband sampling rate in the time domain of $4 \cdot N_{FFT} \cdot \Delta f = 2.5\text{MHz}$. This oversampling in the IFFT reduces the filtering effort still necessary in the up-converter. To make it work, the frame composer is configured to fill up all additional, unused carriers with zeros. At the end of the processing chain, the up-converter then has to numerically interpolate the signal to the desired D/A sampling rate of 30MHz, which means an additional oversampling factor of 12. After this, the actual up-conversion from complex baseband to

real-valued IF is performed by mixing with a numerically controlled oscillator (NCO) running at 10.7MHz. To reduce the implementation effort for the described design, available intellectual property (IP) components were used where possible. For the RS encoder, symbol mapper and IFFT, IP cores from Altera are in use. The up-converter implementation also makes use of Altera IP for the necessary digital interpolation filters and the NCO (cf. Figure 9).

In order to enable the generation of arbitrary sequences of L-DACS1 frames, the processing chain prior to the frame composer needs to handle a number of different configurations for different frames at runtime. Each packet sent into the chain contains a number of configuration bits identifying its frame type and data processing type, whereas each processing block needs a number of parameters specific to that block at its input for each packet. To solve this, a generic processing configuration block has been implemented which contains a small lookup table to translate packet configuration bits into processing parameters. These parameters are then applied to a connected processing block and the data of the incoming packet is routed to the processing block (see Figure 9). Processing results are finally passed on to the next block in the chain, together with the original packet description. This description is held in a FIFO by the configuration block while the packet data is being processed. One instance of this processing configuration block is used for all processing steps prior to the frame composer, except for the zero padder. Zero padder and frame composer are themselves compatible with the employed packet configuration format. The frame composer outputs packets containing one OFDM symbol each. From this stage onwards, all packets can be treated in the same way and configuration bits are no longer necessary, as is also indicated in Figure 9.

As mentioned before, one design goal was to keep components configurable where possible. In the following, the key parameters which can be configured at compile time are outlined for all blocks developed by the authors of this paper. At first, a number of different convolutional codes can be configured for the convolutional encoder, all of which will be supported at runtime. The same is possible for multiple interleaving schemes in the interleaver. Then, a set of multiple frames that the frame composer needs to be able to generate at runtime can be defined at compile time. Each frame is defined by the number and types of header OFDM symbols preceding its data section, by the length in OFDM symbols of that data section, the numbers of subcarriers used in the lower and upper halves of the spectrum during the data section, and the locations and content of pre-defined pilot symbols. Furthermore, the frame composer design allows to disable or enable the insertion of a zeroed DC subcarrier between the lower and upper part of the spectrum and to configure the IFFT length to which an OFDM symbol needs to be filled up with zeroed subcarriers. Finally, any number of samples (in their sum not exceeding the IFFT length) may be configured for the lengths of cyclic prefix and suffix in the blocks responsible for cyclic extension and windowing. The length of the overlap between consecutive OFDM symbols and the windowing function can also be configured at compile time.

An advantage of the frame composer's flexibility is that for the purposes of this implementation, the sequences of header OFDM symbols and tiles appearing in the RL can also be considered frames in a generalized sense. A group of header OFDM symbols is simply a frame with zero OFDM symbols in its data section. The fact that an L-DACS1 TX may be required to transmit only one out of a group of header OFDM symbols and remain silent for the remaining part is handled in the frame composer by setting to zero any combination of header OFDM symbols in a frame. The configuration bits of the corresponding packet determine at runtime which header OFDM symbols will be set to zero. Furthermore, a tile in the RL is a frame with zero header OFDM symbols and a data section that has no used subcarriers either in the lower or upper part of the spectrum. This way, any kind of OFDM symbol sequence which may appear in the L-DACS1 system according to its specification in [3] may be generated with the implementation presented herein.

After compilation in Quartus II, the described implementation together with the interface firmware component shows a resource usage on the Altera Stratix II GX FPGA as indicated in Table 3. Note that the two 512K bit memory blocks are used for the FIFOs of the interface firmware component. These sizes are user-configurable and have been set

Table 3: TX FPGA design resource usage

Resource type	Utilization
Logic elements	25%
512 bit memory blocks	19 / 488
4K bit memory blocks	101 / 408
512K bit memory blocks	2 / 4
DSP block 9-bit elements	80 / 384

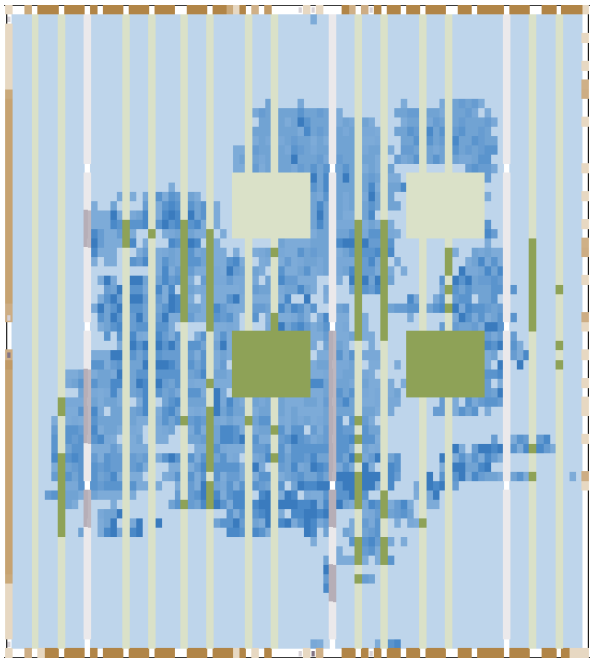

Figure 10: TX in Quartus II Chip Planner.

to such large values for development purposes. Figure 10 shows a graphical representation of the FPGA resource usage generated by the Quartus II Chip Planner feature. Darker areas indicate heavier use while unused areas are lightly colored. Logic elements are depicted in blue, memory in green and DSP elements in grey. The brown squares surrounding the picture are pins.

4.2 Receiver Design in FPGA and Software

As mentioned before, the RX only implements down-conversion and down sampling of the incoming real-valued IF signal, sampled at 30MHz, to an outgoing complex baseband signal sampled at 2.5MHz. This is basically the inverse process to the up-converter in the TX and also makes use of Altera IP cores for its NCO and the necessary decimation filters. The output resolution is 32bits (fixed-point) per complex sample, which leads to a data rate of 10MByte per second on the interface to the host computer. Depending on the available disk space, recordings up to the order of one hour are possible. The recorded data may then be used as input to a software receiver also developed at the German Aerospace Center. This receiver includes all features necessary for operation under realistic channel conditions and severe interference from the DME system as expected in the L-band. Details on its optimization e.g. in terms of interference mitigation and synchronization in the presence of interference may be found in [5] and [6]. An earlier stage of the developed receiver concept is also explained in [2].

At the time of this writing, all described features of TX and RX signal processing were already implemented and working, with the exception of the PTT output signal in the TX. The authors expect to finish implementation of this part shortly.

4.3 RF Frontend

With TX and RX working up to the IF level, the second part that is needed to perform measurements in the L-band is a radio frequency frontend for conversion between the desired L-band TX and RX center frequencies and the IF, as well as for amplification. Especially on the RX side, an RF frontend for L-DACS1 has to perform significant filtering in order to reject signals from other systems operating in the L-band. Additionally, it must achieve a very low noise figure of around 5dB, depending on the performance of the RX algorithm (see noise figure and RX implementation margin assumptions in [3], Annex 1.1). Currently, such a frontend is being developed and built by an external supplier for the German Aerospace Center. It should be available in early May 2010. In order to reduce the effort of such an experimental development, the TX output peak effective power (PEP) will be limited to +27dBm. After subtracting the 12dB of peak-to-average power ratio (PAPR) that the baseband TX signal processing is designed to support, the average TX power in the L-band will be around +15dBm, which is significantly lower than the average power of +41dBm required for L-DACS1 to achieve a range of 120 nautical miles in the en-route scenario [3]. In order to still get realistic experimental results under these

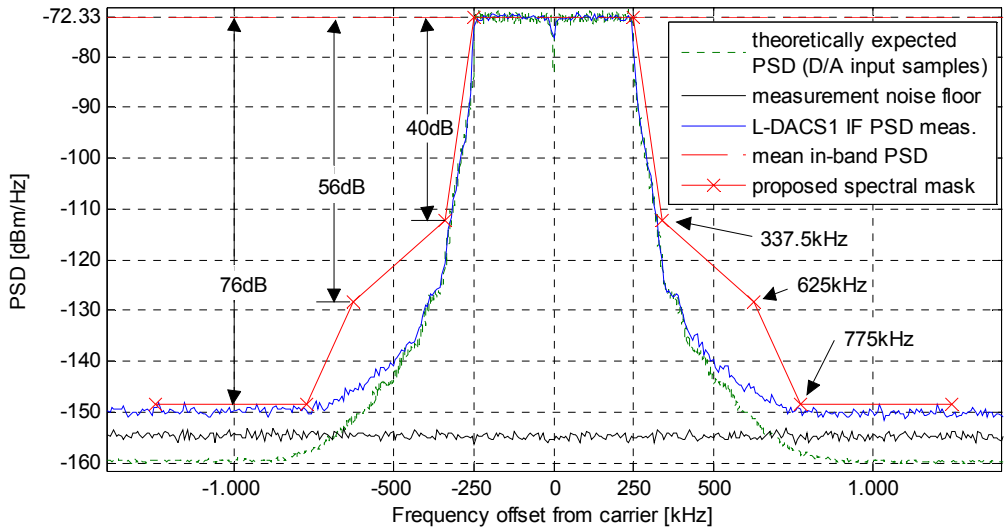

Figure 11: Measured spectrum at IF of 10.7MHz, compared to spectral mask.

conditions, it will be possible to alter the operating point of the final TX amplifier stage to provoke non-linear behavior similar to a real high power amplifier. Moreover, the frontend TX power control will be designed to easily allow the integration of an external high power amplifier into the control cycle at a later time.

5. First Measurements

With the signal processing system and TX FPGA design described above, an L-DACS1 FL TX signal was generated on the IF in a first experimental run. All frames of the repetitive FL Super-Frame structure were filled with random data. For all user data channels, 64-QAM and convolutional code puncturing to a rate of 3/4 was used, while all control channels were encoded without puncturing and modulated using QPSK [3]. Figure 11 shows the measured spectrum at the IF interface. It was recorded by a spectrum analyzer in swept acquisition mode, using a resolution bandwidth of 10 kHz and a video bandwidth of 30 kHz. The displayed result is the power spectral density (PSD) average of 10 sweeps. As indicated in Figure 11, the average in-band PSD is -72.33 dBm/Hz. With an effective signal bandwidth of almost 500 kHz (57 dBHz), a total signal power of about -15.33dBm can be concluded. This is only slightly less than expected based on the D/A board's PEP of -2dBm minus the 12dB of PAPR that the signal processing is designed for. Below the measured IF PSD, the measurement noise floor PSD can be seen. It was measured exactly like the IF signal PSD, this time with the spectrum analyzer's input terminated. As it lies only about 5dB below the measured floor of the IF PSD, it may be assumed that the actual floor of the IF PSD is still somewhat lower. Above the measured IF PSD, the proposed spectral mask for L-DACS1 is shown. It is symmetrical to the carrier frequency and defined by the points marked in Figure 11. The mask is identical to the spectral mask from [3] in all points except the ones at -40 dB from the in-band PSD, which have been moved to an offset of 337.5 kHz from the carrier frequency. This is the current proposal for amendment of the specified spectral mask. As can be seen, the IF signal stays below the spectral mask throughout the out-of-band region beginning at an offset of 250 kHz from the carrier. The room still left between the IF PSD and the shoulders of the mask around the -56 dB points are projected to accommodate the expected third order intermodulation distortion products (IMD3) of a high power amplifier. The fact that the IF PSD stays below the required -76 dB at 775 kHz offset and remains below that level indicates that the L-DACS1 physical layer laboratory demonstrator when combined with its RF frontend will be able to generate L-DACS1 signals in the L-band in compliance with this requirement from [3]. Finally, the theoretically expected IF signal PSD, calculated from a sequence of 14 bit samples as it would usually go to the D/A converter, is also shown in

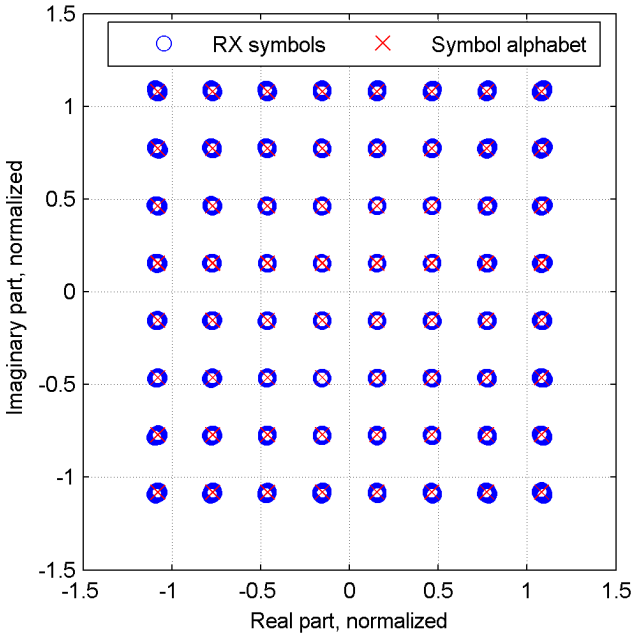

Figure 12: Received 64-QAM constellation.

Figure 11. It has been normalized to have the same power as the IF measurement. The normalized curve matches the IF measurement closely, with the exception of an even lower spectral floor. As displayed, this floor lies about 10dB below the -76dB required by the spectral mask. It does not fall down further as a result of signal quantization.

In a next step, the IF signal for a sequence of ten FL Super-Frames was recorded using the RX signal processing unit and corresponding FPGA design. Again, random data was transmitted with the same coding and modulation settings as before. The recorded complex baseband samples were then processed with the software receiver as outlined in Subsection 4.2. Figure 12 shows all received constellation points for the 64-QAM modulated user data frames (cf. Figure 2), together with the reference points of the modulation symbol alphabet. In total, 781440 64-QAM modulation symbols in 320 frames were processed. The RX modulation symbols were extracted from the receiver after channel estimation and equalization. The relative constellation error root mean square (RMS) was found to be -49.7dB. Furthermore, it could be verified that the received bits were equal to the transmitted bits. These facts, together with the close match between the measured IF PSD and the theoretical PSD shown in Figure 11, demonstrate that the IF signal processing hardware is working correctly.

6. Conclusion and Outlook

With the developed implementation of the L-DACS1 physical layer lab demonstrator, very flexible L-DACS1 transmit and receive components functional up to the IF level are available. Tests at IF level have proven both the functionality of the hardware implementation and the accuracy of the implementation with respect to spectral mask and signal constellation requirements. Together with the RF frontend, the L-DACS1 physical layer lab demonstrator is expected to be ready for first L-band measurements in the May/June 2010 timeframe. Following that, compatibility tests against legacy systems like DME are planned to be carried out at the labs of the German ATC authority DFS. These compatibility tests will include assessments of the interference caused by L-DACS1 on DME similar to those conducted for the Universal Access Transceiver (UAT) [7]. Regarding the robustness of L-DACS1, RX signals impaired by interference from legacy systems will help to verify the system's interference immunity and provide further input to the refinement of receiver algorithms.

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