L-DACS1 LABORATORY DEMONSTRATOR DEVELOPMENT AND COMPATIBILITY MEASUREMENT SET-UP

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Abstract

In this paper, the L-DACS1 physical layer laboratory demonstrator development is described which has been recently carried out by the German Aerospace Center (DLR). The main goal of the lab demonstrator is to perform first compatibility measurements between L-DACS1 and legacy L-band systems where interference from L-DACS1 towards the legacy systems as well as interference from the legacy systems onto the L-DACS1 receiver is considered. In addition to the demonstrator description, results from functional tests of the lab demonstrator as well as the measurement scenarios foreseen for compatibility testing are presented. The compatibility measurements will take place at the labs of the Deutsche Flugsicherung GmbH (DFS) – the German ATC provider – in fall this year.

Introduction

The Future Communications Infrastructure (FCI) comprises a set of data link technologies for aeronautical communications. For the airport, a data link technology dubbed AeroMACS (Aeronautical Mobile Airport Communications System) is currently developed within NextGen and SESAR which is strongly based on the WiMAX standard. ESA initiated the development of a future satellite-based communications system for aviation within the ESA Iris program, supplemented by work performed within SESAR. For air/ground communications, two L-DACS (L-band Digital Aeronautical Communication System) candidates are currently under consideration – L-DACS1 and L-DACS2. Whereas L-DACS1 is a broadband system employing Orthogonal Frequency-Division Multiplexing (OFDM) as modulation scheme and frequency-division duplex (FDD), L-DACS2 is a narrowband single-carrier system utilizing time-division duplex (TDD). The final decision on L-DACS will be based on a set of evaluation criteria including laboratory prototype testing of L-DACS with respect to L-band compatibility.

Current work on L-DACS is performed under the framework of SESAR. The corresponding SESAR project P15.2.4 „Future Mobile Data Link System Definition“ has started activities on L-DACS within an Early Task mid of February this year. Main goals of this Early Task are the refinement of L-DACS specifications, the development of evaluation criteria for L-band compatibility testing, and the set-up for the L-DACS evaluation.

Besides the SESAR activities, the German Aerospace Center (DLR) has already started to implement an L-DACS1 physical layer laboratory demonstrator in FPGA technology based on the current L-DACS1 specification [1]. The demonstrator enables investigations of both the influence of the L-DACS1 waveform on the legacy L-band systems and the interference of the legacy L-band systems on the L-DACS1 receiver. These investigations are especially of interest for the so-called “inlay” deployment scenario, where L-DACS1 and the Distance Measuring Equipment (DME) share the L-band as common spectrum resource by implementing L-DACS1 channels of approximately 500 kHz bandwidth between two adjacent DME channels.

Since the proof of L-band compatibility is the main scope of the DLR demonstrator, the focus is on the physical layer implementation. The demonstrator is implemented in FPGA technology [2] and comprises a complete implementation of the physical layer of the L-DACS1 transmitter, including adaptive coding and modulation as well as the complete framing structure for forward and reverse link. The receiver of the L-DACS1 demonstrator is implemented only partly in hardware. Mainly sampling and digital down-conversion followed by fast data storage are realized, i.e. a data grabber function. The subsequent receiver tasks, like synchronization, interference mitigation, channel estimation/equalization, decoding, and demodulation are realized in software for offline processing of the data gathered by the data grabber function. This concept allows rapid demonstrator set-up and high flexibility for receiver optimization.

The L-DACS1 physical layer laboratory demonstrator is already set-up except for the RF (radio frequency) frontend which has been ordered from an external supplier. An experimental set-up of the RF frontend already exists which is currently tested for gathering data for optimizing the final RF frontend design. The RF frontend delivery is scheduled for October 2010.

Functional tests of the DLR L-DACS1 physical layer demonstrator at an IF (intermediate frequency) of 10.7 MHz, which is used as the interface to the RF frontend, have already been carried out as well as first RF tests using the experimental RF frontend set-up. Functional RF testing will be performed at DLR labs as soon as the RF frontend is delivered. Compatibility testing at the labs of the German ATC provider Deutsche Flugsicherung GmbH (DFS) is currently scheduled for November 2010.

The reminder of the paper is organized as follows. After a brief review of L-DACS1 the demonstrator objectives as well as its implementation in FPGA technology are described. The subsequent sections are devoted to present the already available measurement results of the functional tests. In addition, the measurement scenarios for the planned compatibility testing at DFS labs are described in detail. Finally, some conclusions are drawn and an outlook on further activities is given.

Brief L-DACS1 Review

Using B-AMC (Broadband Aeronautical Multi-carrier Communications System) [3] as baseline design, L-DACS1 resulted from combining B-AMC with the TIA-902 (P34) and the IEEE 802.16e (WiMAX) standards [4]. The B-AMC design resulted from a Eurocontrol funded study on exploring the feasibility of an OFDM-based inlay system for aeronautical communications in L-band.

In the following, the main features and technical characteristics of L-DACS1 are outlined. Please note, L-DACS1 comprises both an Air-Ground (A/G) and an Air-Air (A/A) mode of operation. So far, only the A/G mode has been specified in detail and in this paper, only the A/G mode is considered.

Main Features

L-DACS1 is an OFDM based multi-application data link designed to cover Air Traffic Services (ATS) as well as Airline Operational Communications (AOC). Wide-area coverage is realized by employing a cellular system concept where cell and operational coverage are decoupled. The size of a single cell is adjustable with maximum cell radius of 200 nautical miles (nmi). Handover between cells is seamless, automatic, and transparent to the users.

For the Forward Link (FL) – ground station to aircraft – pure OFDM is chosen, whereas in the Reverse Link (RL) – aircraft to ground station – a combination of Orthogonal Frequency-Division Multiple-Access (OFDMA) and Time-Division Multiple-Access (TDMA) is applied. The TDMA component in RL is crucial to achieve a low duty cycle of L-DACS1 transmissions at the aircraft side to minimize co-site interference towards other onboard receivers. FL and RL are separated by FDD with a duplex spacing of 63 MHz. The effective L-DACS1 bandwidth is 498.05 kHz for both FL and RL. The chosen bandwidth utilizes the frequency gaps between DME channels for the inlay deployment to the maximum extend possible and FDD avoids the necessity to subdivide the 498.05 kHz bandwidth into FL and RL. The frequency ranges for FL and RL for the inlay deployment are foreseen to be 985.5-1008.5 MHz and 1048.5-1071.5 MHz, respectively.

In addition, L-DACS1 supports point-to-point connections as well as broadcast communication (FL only) and offers optionally to set-up voice channels. L-DACS1 is compatible to ATN/OSI and ATN/IPS.

Framing Structure

As shown in Figure 1, the L-DACS1 framing structure is built from super-frames of duration 240 ms. FL and RL super-frames are similar and subdivided into four multi-frames of duration 58.32 ms each and an additional BroadCast (BC) and Random Access (RA) frame, respectively, of duration 6.72 ms. The multi-frames comprise data and control information. In RL, the Dedicated Control (DC) frame is used to request transmission resources and to signal acknowledges, whereas in FL, the Common Control (CC) frame is used to assign

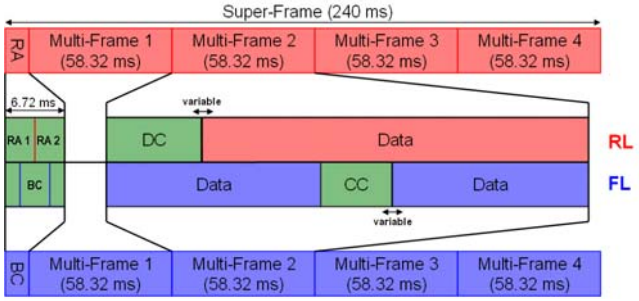

Figure 1: L-DACS1 framing structure.

resources and also to signal acknowledges. The BC frame in FL is used to broadcast cell-specific information and the RA frame in RL is used for the net entry procedure. For a more detailed description of the framing structure, please refer to [1].

Adaptive Coding and Modulation

L-DACS1 adapts to varying quality of the physical channel by supporting a number of Adaptive Coding and Modulation (ACM) options. All applied Forward Error Correction (FEC) coding schemes rely on an outer Reed-Solomon (RS) code followed by a convolutional code of basic rate 1/2 with two optional puncturing schemes to achieve higher convolutional code rates of 2/3 or 3/4. The employed RS code is a systematic code from Galois Field GF(2^3) with a variable number of check symbols and code words shortened to the desired length. The convolutional code polynomials are (171, 133) in octal notation. After coding, the bits of each codeword are interleaved and mapped to modulation symbols using quaternary phase shift keying (QPSK), 16-quadrature amplitude modulation (16-QAM) or 64-QAM. The possible ACM types together with the resulting net data rates assuming a split of 1/9 to 8/9 between control information and data within each multi-frame are shown in Table 1 (upper part: FL, lower part: RL). More details on coding, interleaving, and symbol mapping can be found in [1].

Physical Layer Parameters

The physical layer of L-DACS1 is described by the corresponding OFDM parameters. The central OFDM parameter is the subcarrier spacing which for L-DACS1 is chosen to be 625/64 = 9.765625 kHz. On the one side, this bandwidth is large enough to avoid inter-carrier interference due to Doppler effects

Table 1: ACM types and resulting net data rates

Modulation	Code Rate (conv. code)	RS Code Parameter	Total Code Rate	Resulting Data Rate
QPSK	1/2	RS(110, 91, 5)	0.45	291 kbit/s
QPSK	2/3	RS(134, 120, 7)	0.60	384 kbit/s
QPSK	3/4	RS(151, 135, 8)	0.67	432 kbit/s
16-QAM	1/2	RS(202, 182, 10)	0.45	582 kbit/s
16-QAM	2/3	RS(135, 121, 7)	0.60	774 kbit/s
64-QAM	1/2	RS(152, 136, 8)	0.45	870 kbit/s
64-QAM	2/3	RS(203, 183, 10)	0.60	1171 kbit/s
64-QAM	3/4	RS(228, 206, 11)	0.68	1318 kbit/s

Modulation	Code Rate (conv. code)	RS Code Parameter	Total Code Rate	Resulting Data Rate
QPSK	1/2	RS(16, 14, 1)	0.44	270 kbit/s
QPSK	2/3	RS(21, 19, 1)	0.60	364 kbit/s
QPSK	3/4	RS(24, 22, 1)	0.69	422 kbit/s
16-QAM	1/2	RS(32, 28, 2)	0.44	537 kbit/s
16-QAM	2/3	RS(43, 39, 2)	0.60	748 kbit/s
64-QAM	1/2	RS(49, 45, 2)	0.46	864 kbit/s
64-QAM	2/3	RS(66, 60, 3)	0.61	1153 kbit/s
64-QAM	3/4	RS(74, 66, 4)	0.67	1267 kbit/s

and, on the other side, it is small enough to guarantee flat fading within the subcarrier bandwidth and with that allows the usage of a simple channel equalizer structure at the receiver. The useful OFDM symbol time – the reciprocal of the subcarrier spacing – is 102.4 µs which is extended to the OFDM symbol time of 120 µs by adding a cyclic prefix of duration 17.6 µs. The cyclic prefix consists of a guard time of 4.8 µs to avoid inter-symbol interference caused by echoes and another 12.8 µs for windowing to improve spectral characteristics. OFDM modulation/demodulation is performed by an Inverse Fast Fourier Transform (IFFT) and Fast Fourier Transform (FFT) of length 64, respectively. The overall IFFT/FFT bandwidth is 625 kHz. However, since only 50 subcarriers are used for transmission – 25 subcarriers left and right of the unused DC subcarrier – the effective L-DACS1 bandwidth reduces to 498.05 kHz. The main OFDM parameters

defining the L-DACS1 physical layer are summarized in Table 2. For more details on the L-DACS1 physical layer, please refer to [1].

Table 2: Main OFDM parameters of L-DACS1

OFDM Parameter	Value
FFT size	64
Number of used subcarrier	50
Subcarrier spacing	9.765625 kHz
Useful symbol time	102.4 µs
Sampling time	1.6 µs
Cyclic prefix ratio	11/64
Cyclic prefix	17.6 µs
OFDM symbol time	120 µs
Guard time	4.8 µs
Windowing time	12.8 µs
Window roll-off factor	0.107
Total FFT bandwidth	625 kHz
Effective bandwidth	498.05 kHz

Demonstrator Objectives

The objectives of the demonstrator development are twofold. First, the effects of L-DACS1 signals on existing systems in the L-band are to be analyzed using a realistic setup, i.e. actual hardware. This will allow to establish the conditions under which coexistence of L-DACS1 with such systems is possible, for example the necessary spatial and spectral separation. Secondly, the robustness of L-DACS1 against interference from other systems is to be demonstrated and assumptions regarding the bit error rate (BER) and minimum required signal level have to be proven.

In order to achieve this, the transmitter (Tx) has to be able to generate all L-DACS1 frame types for the FL and RL. It should be able to output any sequence composed of the above types of signals that will also occur in the final L-DACS 1 system. Furthermore, support of all ACM options defined in [1] is desired. For later comparison of transmitted and received data, i.e. BER evaluation, it has to be possible to fill transmit sequences with arbitrary, predefined data, e.g. read from a file. In order to facilitate accurate BER measurements, large amounts of user data have to be transmitted in an automated way in one experiment, e.g. all in one long sequence.

In the L-DACS1 specification [1], the receiver (Rx) algorithm is not defined in detail, and can thus be considered implementation-specific. Depending on how exactly the system will be deployed in the L-band [5], the Rx will have to operate under significant interference conditions. As the deployment concept has not yet been decided and so far, only theoretical analysis of the interference has been done, no detailed interference model is available. Therefore, the demonstrator's Rx signal processing must stay flexible and easy to adapt to refined Rx algorithms. This can be achieved by implementing as much of it as possible in software. The hardware part only has to implement filtering and down-conversion into complex (I/Q) baseband samples, which can then be stored, e.g. on the hard disk of a host computer, to allow later software processing. Similar to the Tx, the Rx should be able to record long, continuous sequences for the purpose of accurate BER measurements. The output of such a data grabbing Rx can also be a great aid in the development and testing of new Rx algorithms.

As the development of the described L-DACS1 demonstrator began prior to the finalization of the L-DACS1 specification, a further design goal was to keep the implementation of all signal processing components as flexible as possible, in order to allow easy parameter modification (e.g. framing structure, coding parameters). Another reason for this is the planned re-use of as much of the implementation as possible in a data link for research aircraft of DLR.

Demonstrator Implementation

The L-DACS1 physical layer laboratory demonstrator consists of signal processing units for Rx and Tx, as well as of a radio frequency (RF) frontend, see Figure 2. The main interface between those stages consists of the analogue Tx and Rx signals on an intermediate frequency (IF) of 10.7 MHz, down-converted from the L-band and amplified by the frontend for Rx and delivered to the frontend for Tx.

For the purpose of signal processing in experimental implementations, two identical FPGA-

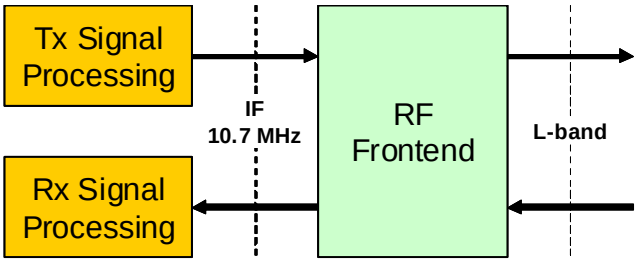

Figure 2: L-DACS1 lab demonstrator set-up.

based systems have been purchased by DLR from an external supplier. As shown in Figure 3, the compact-PCI platforms contain a host PC, two processing boards, a digital to analogue (D/A) converter board and an analogue to digital (A/D) converter board. The processing boards rely on an Altera Stratix II GX FPGA for arbitrary user designs. Memory is also provided, together with hardware, firmware and software for a PCI interface between boards and the host computer. This interface provides software functions for sending data from the host to a board and vice-versa. On the processing FPGA, by an already existing firmware component, data from the host computer is made available via an Avalon-Streaming (AVST) interface [6], which in this case can be thought of as a first in first out (FIFO) memory. This interface firmware component also accepts data via AVST and transfers it to the host where it is available through the software functions. Furthermore, it is possible to setup data streams from a processing board to the D/A converter board and from the A/D converter board to a processing board.

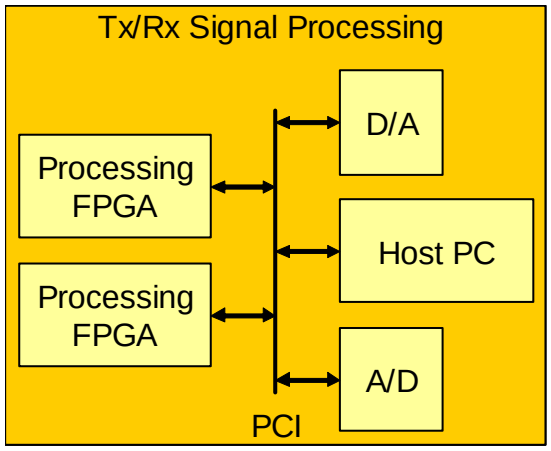

Figure 3: Signal processing system.

The D/A and A/D converters both support 2 channels with a resolution of 14 bits. The maximum conversion rates supported are 150 MHz and 105 MHz for D/A and A/D, respectively. For the L-DACS1 demonstrator, the sampling clocks have both been set to 30 MHz, which is sufficient for the desired IF and signal bandwidth. This reduction minimizes the necessary bandwidth between processing boards and converter boards. Image rejection in the Tx is no problem at this sampling rate because the employed D/A converter chip internally performs a numerical interpolation to two times the input rate. The Stratix II FPGAs on the processing boards are clocked at 100 MHz.

Both the transmitter and receiver implementation is described in detail in [2] and summarized in the following two subsections.

Transmitter Implementation

The transmitter signal processing FPGA design that had to be implemented for the physical layer laboratory demonstrator receives AVST packets at its input containing all parameters and data for a sequence of L-DACS1 frames. This is enabled by the AVST interface firmware of the signal processing systems. From the received packets, the aforementioned IF signal has to be generated, along with an envelope signal and an activation signal for the RF amplifier. The envelope signal is needed by the frontend for accurate Tx power control. The generated signals have to be sent back to the AVST interface firmware, which for the Tx has to be configured to transmit data to the D/A board. To accomplish these tasks, functional blocks are connected via AVST into a processing chain [2]. As a consequence, arbitrary sequences of L-DACS1 frames – FL and RL – can be realized by this transmitter implementation.

The concept used in terms of sampling rate relies on a four-times oversampling in the IFFT with respect to the nominal transform length of 64 as specified in Table 2, which leads to a transform length for implementation of 256 and a complex baseband sampling rate in the time domain of 2.5 MHz. This oversampling in the IFFT reduces the filtering effort still necessary in the up-converter. To make it work, the frame composer is configured to fill up all additional, unused carriers with zeros. In addition, the up-converter has to numerically

interpolate the signal further to the desired D/A sampling rate of 30 MHz, which means an additional oversampling factor of 12. After this, the actual up-conversion from complex baseband to real-valued IF is performed by mixing with a numerically controlled oscillator (NCO) running at 10.7 MHz.

The effort for the described transmitter implementation could be reduced by using available intellectual property (IP) components. For the RS encoder, symbol mapper and IFFT, IP cores from Altera have been used. The up-converter implementation also makes use of Altera IP for the necessary digital interpolation filters and the NCO.

Receiver Implementation

As mentioned before, the Rx only implements down-conversion and down sampling of the incoming real-valued IF signal, sampled at 30 MHz, to an outgoing complex baseband signal sampled at 2.5 MHz. This is basically the inverse process to the up-converter in the Tx and also makes use of Altera IP cores for its NCO and the necessary decimation filters. The output resolution is 32 bits (fixed-point) per complex sample, which leads to a data rate of 10 MByte per second on the interface to the host computer. Depending on the available disk space, recordings up to the order of one hour are possible. The recorded data may then be used as input to a software receiver also developed at DLR. This receiver includes all features necessary for operation under realistic channel conditions and severe DME interference as expected in the L-band. Details on its optimization e.g. in terms of interference mitigation and synchronization in the presence of interference may be found in [7] and [8].

RF Frontend

With Tx and Rx working up to the IF level, the second part that is needed to perform measurements in the L-band is a radio frequency frontend for conversion between the desired L-band Tx and Rx center frequencies and the IF, as well as for amplification. Especially on the Rx side, an RF frontend for L-DACS1 has to perform significant filtering in order to reject signals from other systems operating in the L-band. Additionally, it shall achieve a very low noise figure of around 5dB (Annex 1.1 in [1]), depending on the performance of the Rx algorithm. Such a frontend has been specified and ordered by DLR from an external supplier. Delivery is currently scheduled for October 2010.

In order to reduce the effort of such an experimental development, the Tx output peak effective power (PEP) will be limited to +27 dBm. After subtracting the 12 dB of peak-to-average power ratio (PAPR) that the baseband Tx signal processing is designed to support, the average Tx power in the L-band will be around +15 dBm, which is significantly lower than the average power of +41 dBm required for L-DACS1 to achieve a range of 120 nmi in the en-route scenario [1]. In order to still get realistic experimental results under these conditions, it will be possible to alter the operating point of the final Tx amplifier stage to provoke non-linear behavior similar to a real high power amplifier. Moreover, the frontend Tx power control will be designed to easily allow the integration of an external high power amplifier into the control cycle at a later time.

Functional Tests

Functional tests of the L-DACS1 laboratory demonstrator are performed to prove proper working of the baseband signal processing and the digital up-/down-conversion to/from IF. In addition, first RF tests using the experimental RF frontend set-up are carried out. In both cases, the focus of the functional tests is on the transmitter spectral mask and the behavior of the overall transmission chain. In Figure 4, the set-up for the functional tests is depicted.

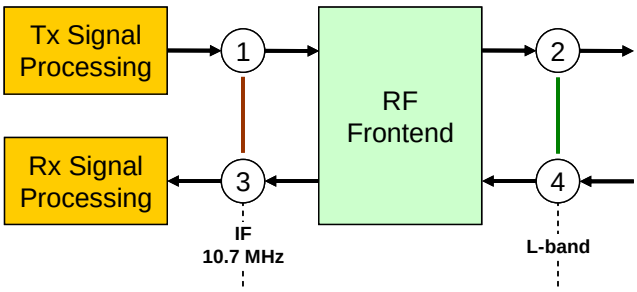

Figure 4: Set-up for the functional tests.

The transmitter spectral mask for IF and RF can be measured with a spectrum analyzer connected to measurement point 1 or 2, respectively. Connecting the points 1 and 3, an IF loop is realized and the transmission chain in IF loop can be verified. Correspondingly, connecting points 2 and 4 creates

an RF loop for testing the transmission chain in RF loop.

For the functional tests, an L-DACS1 FL Tx signal is generated and up-converted to IF and RF, respectively. All frames of the repetitive FL super-frame structure are filled with random data. For all user data channels, the most challenging ACM scheme – 64-QAM with convolutional code puncturing to a rate of 3/4 – is used, while all control channels are encoded without puncturing and modulated using QPSK.

In the following, the measurement results for the transmitter spectral mask and the overall transmission chain for the IF loop are reported as already presented in [2]. In addition, preliminary results obtained for the RF loop are presented based on the experimental RF frontend set-up.

Transmitter Spectral Mask

The transmitter spectral mask is recorded by a spectrum analyzer in swept acquisition mode, using a resolution bandwidth of 10 kHz and a video bandwidth of 30 kHz. The displayed result is the power spectral density (PSD) average of 10 sweeps.

IF Measurements

In Figure 5, the results from the IF measurements are depicted. As can be seen, the average in-band PSD is -72.33 dBm/Hz. With an effective signal bandwidth of almost 500 kHz (57 dBHz), a total signal power of about -15.33dBm can be concluded. This is only slightly less than expected based on the D/A board's PEP of -2dBm minus the 12dB of PAPR that the signal processing is designed for. Below the measured IF PSD, the measurement noise floor PSD can be seen. It has been measured exactly like the IF signal PSD, with the spectrum analyzer's input terminated. As it lies only about 5dB below the measured floor of the IF PSD, it may be assumed that the actual floor of the IF PSD is still somewhat lower. Above the measured IF PSD, the proposed spectral mask for L-DACS1 is shown. It is symmetrical to the carrier frequency and defined by the points marked in Figure 5. As can be seen, the IF signal stays below the spectral mask throughout the out-of-band region beginning at an offset of 250 kHz from the carrier. The room still left between the IF PSD and the shoulders of the mask around the -56 dB points are projected to accommodate the expected

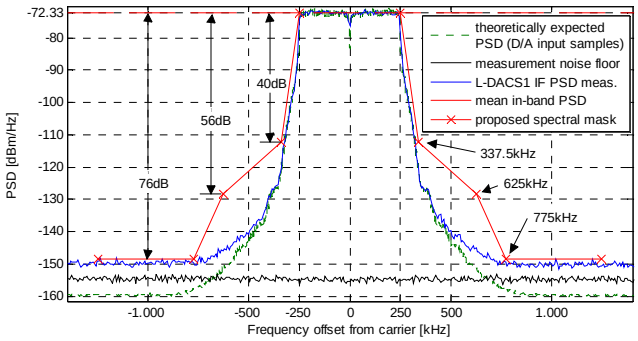

Figure 5: Spectral mask measurement (IF).

third order intermodulation distortion products (IMD3) of a high power amplifier. The fact that the IF PSD stays below the required -76 dB at 775 kHz offset and remains below that level indicates that the L-DACS1 physical layer laboratory demonstrator, when combined with its RF frontend, will be able to generate L-DACS1 signals in the L-band in compliance with the spectral mask. Finally, the theoretically expected IF signal PSD, calculated from a sequence of 14 bit samples as it would usually go to the D/A converter, is also shown in Figure 5. It is normalized to have the same power as the IF measurement. The normalized curve matches the IF measurement closely, with the exception of an even lower spectral floor. As displayed, this floor lies about 10dB below the 76 dB required by the spectral mask. It does not fall down further as a result of signal quantization. As a result, the transmit spectrum of the hardware generated L-DACS1 signal at IF matches very well with the theoretical curve and complies with the proposed spectral mask for L-DACS1.

Preliminary Results Obtained With Experimental RF Frontend

In Figure 7, the preliminary results from the RF measurements are shown which are obtained based on the experimental RF frontend set-up. For this measurement, the transmit power of the experimental RF frontend is set to +10 dBm. Although not yet optimized the experimental RF frontend already complies with the slopes of the spectral mask. Only the noise floor is currently too high and should be reduced by around 15 dB in the final design. However, this is not seen as a problem by our external supplier. Thus, it is expected that the final RF frontend design also complies with the spectral mask as requested by the L-DACS1 specification.

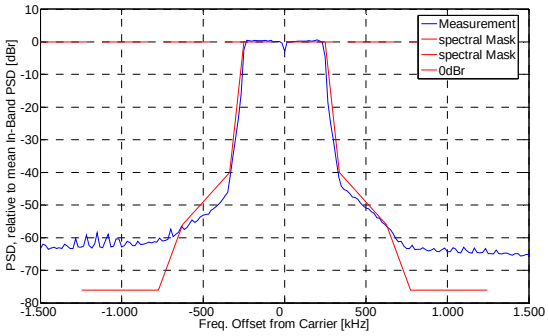

Figure 7: Spectral mask measurement (RF).

Transmission Chain

For testing the overall transmission chain, the received signal for a sequence of ten FL super-frames is recorded using the Rx signal processing unit and corresponding FPGA design. The recorded complex baseband samples are processed off-line with the L-DACS1 software receiver.

IF Measurements

Figure 7 shows all received constellation points for the 64-QAM modulated user data frames together with the reference points of the modulation symbol alphabet. In total, 781440 64-QAM modulation symbols are processed. The Rx modulation symbols are extracted from the receiver after channel estimation and equalization. The relative constellation error root mean square (RMS) is found to be -49.7 dB. Furthermore, it is verified that the received bits are equal to the transmitted bits. These facts demonstrate that the overall transmission chain in IF loop is working correctly.

Preliminary Results Obtained With Experimental RF Frontend

The measurement of the overall transmission chain previously performed for the IF loop is repeated for the RF loop using the experimental RF frontend set-up. As a result, a relative constellation error RMS of -27.9 dB is reported for this RF loop measurement. Of course, this result is considerable worse than the previous result obtained for the IF loop measurement, since the phase noise of the local oscillators (LOs) of the RF frontend increase the constellation error. In [1], the maximum allowed constellation error for QPSK is defined and set to -15 dB. That is well achieved by the current RF frontend design. However, considering requirements for

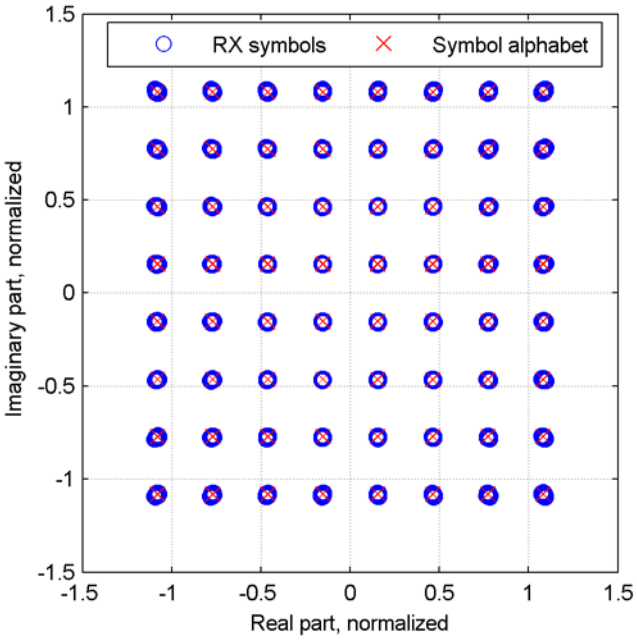

Figure 6: Received 64-QAM signal constellation.

higher signal constellations, like 16-QAM or 64-QAM, the maximum allowed constellation error should be considerably lower than -15 dB. In the WiMAX standard, for example, for 16-QAM and rate ¾ coding, -25 dB are requested and for 64-QAM and rate ¾ coding even -31 dB. As can be seen from that, the current constellation error produced by the experimental RF frontend is sufficient for 16-QAM, but has to be improved for 64-QAM by approximately 3 dB. This important result from the preliminary RF frontend measurements has been reported to the RF frontend supplier who is now adapting the LO mixing concept in order to improve the phase noise and with that the constellation error by at least 3-4 dB.

Compatibility Measurement Set-up

Considering the interference from the DME system, different scenarios can be defined distinguishing between a ground and an airborne interfering and victim system [9]. However, the goal of the laboratory assessment is to derive some general co-existence conditions. The results obtained should reveal the minimum separation needed between these two systems in different environments, taking into account not only the path loss, but also antenna characteristics and cable losses. Generating and evaluating interference of only one DME system

in dependence on frequency offset between DME and L-DACS1 would also enable to verify the software tool for interference simulations, which then can be extended to simulate the impact of a composite interference from multiple aircraft and ground stations.

For all defined measurement cases, the frequency offset between the interfering and victim system should be varied from the worst-case frequency spacing of 500 kHz to the first channel separation where the interference impact is negligible.

Due to differences in DME transponder and interrogation signal [9] as well as their performance requirements [10], laboratory tests should imply both, DME ground and airborne units. Similarly, L-DACS1 settings will differ in forward- and reverse link. The resulting test cases are described in the following.

Test Cases

In the following, three different test cases are described comprising L-DACS1 receiver sensitivity and the mutual impact between L-DACS1 and DME.

L-DACS1 Receiver Sensitivity Test

Receiver sensitivity of the L-DACS1 demonstrator may differ from the requirements defined in [1]. The minimum power level at the L-DACS1 receiver that provides the required BER performance is used as an operating point when testing the impact of the DME system. Hence, BER versus L-DACS1 transmit power should be evaluated prior to the interference measurements in order to test the performance and determine the sensitivity of the deployed L-DACS1 receiver. Since the BER performance depends on type and length of the chosen FEC code, all different frame types have to be considered for the BER measurements. For FL, BER measurements separately for CC and Data frames have to be performed, whereas for RL separate BER measurements for DC frames and user data consisting of different number of tiles are required.

DME Impact on L-DACS1

To determine the impact of DME signals on the L-DACS1 receiver, a fully attenuated DME signal is fed into the L-DACS1 receiver operating at sensitivity level. The attenuation is decreased until the interference power at the victim receiver causes a non-acceptable L-DACS1 performance. The following measurement cases should be evaluated:

- DME airborne interrogator interference on L-DACS1 ground receiver, recording the BER versus the interference level (DME transmit power and attenuation setting). This measurement has to be repeated for different frequency offsets and for all different RL frame types.
- DME ground transponder interference on L-DACS1 airborne receiver recording the BER versus the interference level. This measurement has to be repeated for different frequency offsets and for all different FL frame types.

L-DACS1 Impact on DME

After verifying sensitivity of the DME testing units, the L-DACS1 impact on DME operating at the sensitivity level should be evaluated. L-DACS1 duration of transmission T_{RL} and duty cycle t_d in RL are adjustable test parameters when considering an airborne L-DACS1 transmitter. Starting from the minimum frame duration of 0.72 ms, the frame duration should be increased in steps of 0.72 ms until the maximum allowed duty cycle is reached. Beside the chosen parameter settings (T_{RL}, t_d), the general cases to be distinguished are:

- L-DACS1 interference caused by RL transmission on DME ground transponder receiver, recording Beacon Reply Efficiency (BRE) [10] versus interference level. For this case, different (T_{RL}, t_d) parameter sets have to be considered.
- L-DACS1 interference caused by FL transmission on DME airborne interrogator receiver, recording the Break Stable Operating Point (BSOP) [10], i.e. the L-DACS1 interference power where the DME looses track. Starting from the BSOP, the L-DACS1 interference power is then decreased recording the Acquire Stable Operating Point (ASOP) [10], i.e. the maximum interference power where the DME is able to acquire a track again.

Note, in the latter case only FL transmissions are considered, although other aircraft contribute to the L-DACS1 interference on the DME airborne interrogator receiver. The interference from other aircraft is caused by RL transmissions and, thus, not

continuous like the FL transmission. Therefore, the FL transmission is considered more severe.

Conclusions

The developed L-DACS1 physical layer laboratory demonstrator is designed for the compatibility measurements which are required to prove possible co-existence between L-DACS1 and the L-band legacy systems and to determine the conditions under which such co-existence is achieved. The L-DACS1 laboratory demonstrator is already implemented up to IF level with the RF front-end being currently optimized. Functional tests at IF level prove the proper working of the baseband unit, whereas preliminary RF tests indicate that the final demonstrator is capable of fulfilling the L-DACS1 specifications.

Functional testing at RF level of the finalized L-DACS1 laboratory demonstrator will be carried out at DLR labs after delivery of the final RF frontend version in October 2010. Compatibility testing at the labs of the German ATC provider Deutsche Flugsicherung GmbH (DFS) is scheduled for November 2010.

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